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Design and Analysis for Low power CMOS Sram cell in 90nm technology using cadence tool

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Abstract: CMOS RAM Cell is very less power consuming and has very less read and writes time. As the technology is improving channel length of MOSFET is scaling down. In this environment stability of SRAM becomes the major concern for future technology. A SRAM cell must meet requirements for operation in submicron/nano ranges. So we have to modify conventional 6T SRAM circuit with additional circuitry and different kind of parametric analysis can be done and functionality is verified using Cadence Design Environment for 90nm technology files.

Keywords: SRAM, Cadence virtuoso, 90nm Technology.

I. INTRODUCTION

SRAMs have become a critical component of many VLSI chips. This is especially true for microprocessors, where the on-chip cache sizes are growing with each generation to bridge the increasing divergence in the speeds of the processor and the main memory. Simultaneously, power dissipation has become an important consideration both due to the increased integration and operating speeds, as well as due to the explosive growth of battery operated appliances Static Random access memory (SRAM) is an important functional element in most modern semiconductor products.

II. DESIGN OF CONVENTIONAL 6T SRAM CELL

6T SRAM cell each bit in SRAM is stored on four transistors that form two cross coupled inventor. This storage cell has two stable states which are used to denote 0 and 1. Two additional access transistors serve to control access to storage cell during read and write operation. [1] Access to the cell is enabled by the word line which controls the two access transistor which in term control, whether the cell should be connected to the bit line BL and BL BAR. [2] They are used to transfer data for both read and write operations. An SRAM cell has three different states it can be in: standby where the circuit is idle, reading when the data has been requested and writing when updating the contents. The SRAM to operate in read mode and write mode should have "readability" and "write stability" respectively. [3, 4]

The 6-T SRAM cell operates as follows:

(1) For a read operation, Basic condition is that the strength (drive current) of the pull-down transistor to that of the pass-gate transistor should be sufficiently large. It is called cell Beta ratio. The bit-lines are usually *pre-charged*

To a high level (VDD) and then the word-line is selected (pulsed to a high level). On the side of the cell storing a Logical '0' (*i.e.*, a low Voltage), the bit line is discharged via the pass-gate transistor and pull-down transistor, so that a differential voltage develops between the bit-lines. This differential voltage should be large enough for a sense amplifier to detect the state of the cell. The differential voltage should not be too large, however; otherwise the cross-coupled inverters could flip their state.

(2) For a write operation, Basic condition is that the ratio of the strength of the pass-gate transistor to that of the pull-up transistor should be sufficiently large. It is called cell *gamma ratio.* The bit-lines are driven to complementary voltage levels via a write driver and then the word-line is selected. On the side of the cell for which the bit-line voltage is logical '0' (*i.e.*, a low voltage), the internal storage node is discharged through the pass-gate transistor. The cross-coupled inverters raise the voltage on the opposite storage node and latch the cell. The discharging strength of the pass-gate transistor must overcome the restoring strength of the pull-up transistor.

(3) For a Standby Operation, Basic condition is that the word line is not asserted, the access transistors N3 and N4 disconnect the cell from the bit lines. The two cross

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coupled inverters formed by P1-N1, P2-N2 will continue to reinforce each other as long as they are connected to the supply.

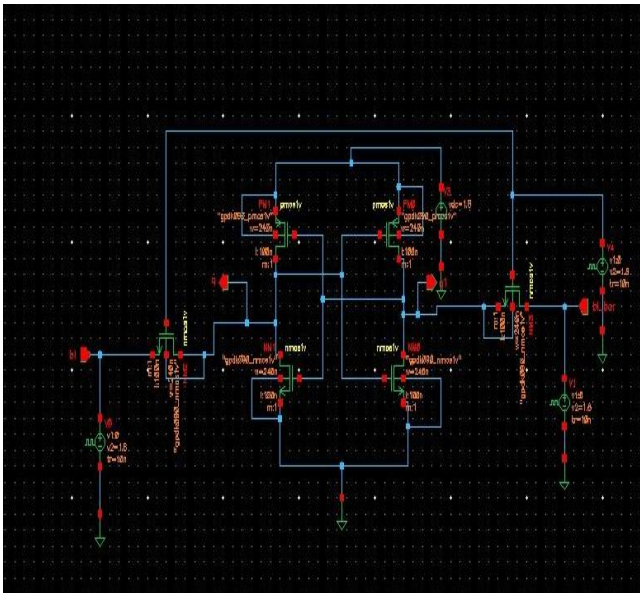

Fig. 1 6T-cell Schematic in Cadence virtuoso.

III. MODIFIED 6-T STATIC RAM CELL WITH SENSE AMPLIFIER

In Conventional 6T SRAM Cell is a limitation can be overcome with modified 6T static ram cell with sense amplifier. The sense amplifier to detect the voltage different on the bit lines is shared by multiple bit lines and connection of the sense amplifier to a bit line pair is controlled by a column selection line. During a read operation, the selected latch outputs the stored value onto the two bit-lines. Since the bit-lines are always recharged, the bit-line differential voltage degrades. We use sense amplifiers to improve the differential voltage from the bit-lines. The main advantage in using a differential bit-line is common-mode rejection, which reduces noise effects and signal degradation. A cross-coupled amplifier is used for the sense amp. Once a memory cell is selected for the read operation, the voltage on one of the complementary bit lines will start to drop slightly.

Suppose that bit+ is higher than bit-. As a result, one of the NFETs, M3, is turned on, causing sense- to be pulled low. Consequently, one of the PFETs, M2, is turned on, pulling up sense+ output to a high value. The positive feedback of the cross-coupled PFETs accelerates the sensing speed by reinforcing M2's gate value (sense-) to a high through M3. The sense amplifier is the key component that limits the speed of read-time. Since the transistor sizing affects the speed of the sense amplifier.

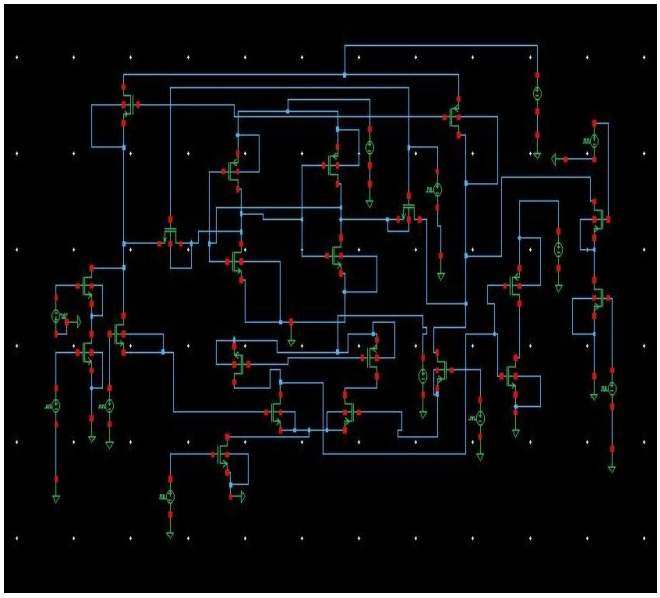

Fig. 2 6-T SRAM Cell with Sense Amplifier.

Schematic circuit diagram with Cadence Virtuoso software is used in sense amplifier 6T SRAM cell.

The transistors NMOS_3, PMOS_4 and NMOS_2, PMOS_1 form cross coupled inverters. For Conventional 6T SRAM Cell, We change Different width of access transistor and pull down transistor and pull up transistor. So read and write operation can be done.

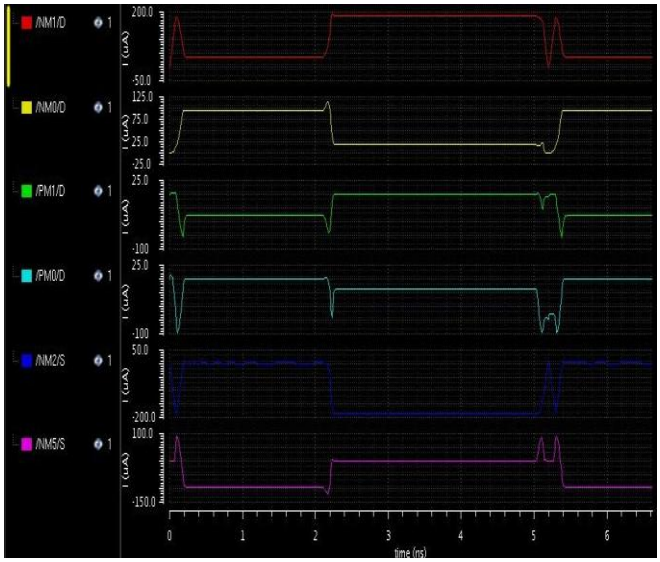

Fig. 3 Current waveforms of Read '0' operation (for conventional 6-T cell).

Schematic Fig. shows current wave form for two access transistor and four cross coupled inverter. Access transistor measured current at source terminal and cross coupled inverter at drain terminal.

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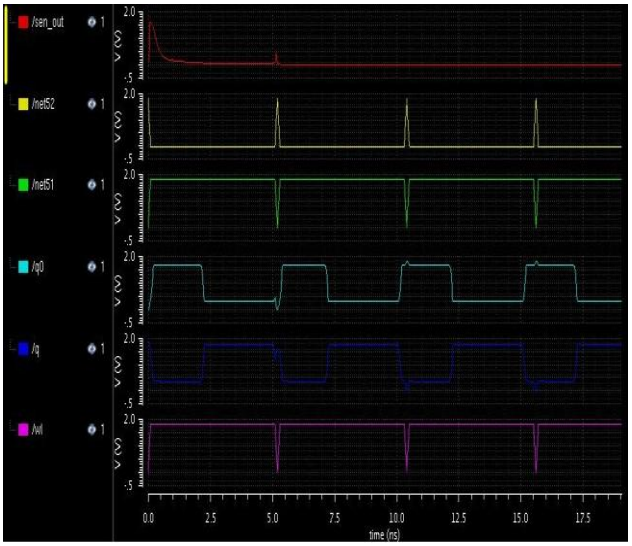

Fig. 4 Word line and Bit line Wave form for Read Zero Operation.

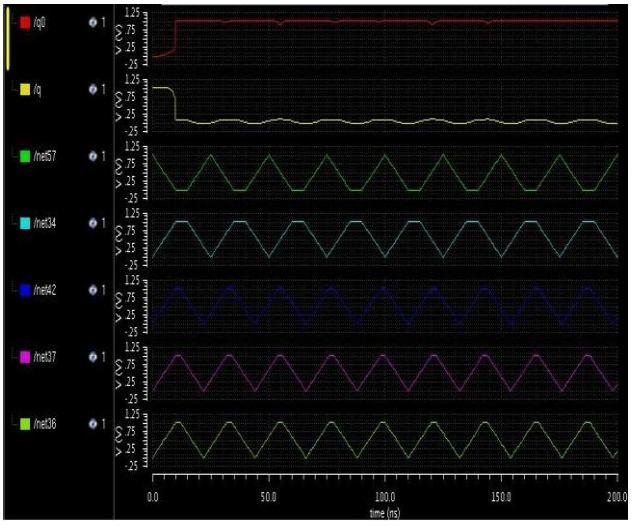

Fig. 5 Schematic of Write Operations

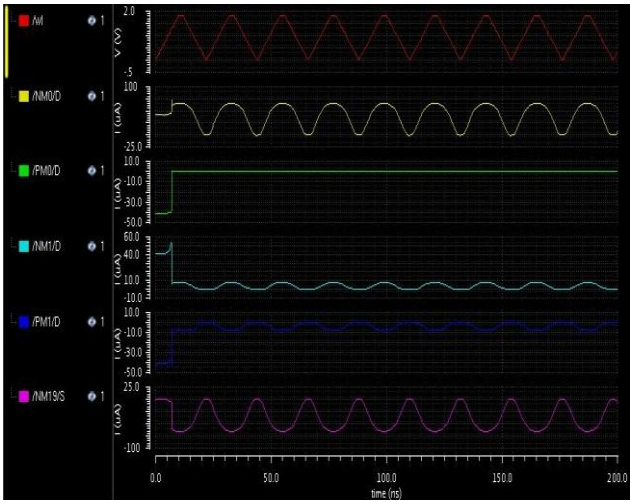

Fig. 6 Current waveforms of Read '1' operation (for conventional 6-T cell).

IV. POWER DISSIPATION OF 6T SRAM CELL WITH SENSE AMPLIFIER

Power dissipation is defined as the rate of energy transfer, Power dissipation or lost from electrical system. When an electrical current does not work on a conductor the internal energy of the conductor increase causing its temp. To rise above the ambient temp. The total power dissipation of a circuit includes both a dynamic and a static component that can be challenging to isolate from each other in simulations.

Dynamic power dissipation: Dynamic power dissipation is further classifies into two categories, namely short circuit power and power consumption during switching. Dynamic power dissipation classified in to two categories.

(A) Short circuit power: As if the input signals are having finite slopes which causes direct-path currents to flow through the gate for a short time during switching operation. For this short duration of time, there exists a direct path between V_{DD} and GND and circuit consumes large amount of power. From the figure 2 the energy consumed per switching is calculated as below

$E_{dp} = V_{dd} \times I_{peak} \times T_{sc}$..... (1)

$P_{shortcut} = V_{dd} \times I_{peak}$..... (2)

Where,
V_{dd} = Voltage supply
Ipeak = Peak current
t_{sc} = time period of power consumption

Matching the rise and fall times of the gate will results in reduced short circuit power. In practice, however, the times are not matched, since optimizing for propagation delay can result in unmatched times. So circuit power is also a major source of power consumption in the digital circuit.

(B) Power Consumption during Switching: Charge is moved from V_{dd} to the output of the inverter, during and after input transaction, hereby pulling V_{out} to V_{dd}. The lumped capacitance C_L results from parasitic wire capacitances and from gate capacitances of the logic gates driven by the inverter. the opposite transition of the input, the PMOS transistor switches off and the NMOS transistor switches on. Now the charge stored on C_L is moved to ground. This output capacitances consumed the power during switching is known as the dynamic power dissipation. It is the largest source of energy dissipation in CMOS circuit. In summary, one rising and the following falling transition of the output consume energy of

$E = C_{load} \times V_{dd} \times V_{dd}$..... (3)

Where
C_{Load} is the load capacitance
V_{dd} is the Power supply

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If f is the clock frequency and the average number of low to high or high to low transitions (the switching activity) of the node is denoted by α then the power consumption due to capacitive switching is given by

$$P_{switching} = \alpha C_{load} (V_{dd})^2 f \ldots\ldots\ldots\ldots (4)$$

Where
α = activity factor
V_{dd} = voltage swing of the output node
C_{Load} = effective capacitance of the output load
f = switching frequency

Static power dissipation: we simply apply a static (DC) input signal so that no switching occurs. For digital circuits, these amounts to a high (VDD) or low (ground) at the input, this typically turns one side of the circuit off and eliminates any static short circuit current through the transistors. For analog circuits, the input should be set to the appropriate DC operating point of the circuit, typically somewhere between ground and VDD. This is one of the reasons that analog circuits consume more power; in their static state many transistors are turned on and consume static power.

Temperature VS Power Dissipation: For calculation of power, temperature is varied from 0c to 50c as shown in table1 and corresponding power dissipation is noted down. As temperature increase power dissipation also increase. The Profile of power Dissipation for the cells shown for different value of temperature at 90nm technology modified 6T SRAM cell with sense amplifier power dissipation higher compared conventional 6Tcell.

TABLE 1 Temperature VS Power Dissipation

Temperature	Power Dissipation (uw)
0^0 C	56.8861
10^0 C	58.4086
27^0 C	64.7452
50^0 C	78.5531
70^0 C	92.6890

Supply Voltage VS Power Dissipation: For calculation of power supply voltage v_{dd} is varied from 1.8 to 1.0 and corresponding power dissipation needs. As supply voltage increase power dissipation also increase.

TABLE 2 Supply Voltage VS Power Dissipation

Supply Voltage	Power Dissipation (uw)
1.0	24.14
1.2	34.92
1.4	40.18
1.5	60.34
1.8	80.63

V. CONCLUSION

In this paper, power analysis of modified 6T SRAM cell with sense amplifier by varying temperature and supply voltage has been done and result are compared with conventional 6T sram cell as temperature increase power dissipation increase and same as supply voltage increase power dissipation also increase. The simulation results using cadence tool much better performance achieve using modified 6T SRAM cell with sense amplifier.

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